Value-added course on

Advances in Packaging for Wide Band Gap Devices

by
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Organized by the Departments of Power Engineering and Instrumentation & Electronics Engineering
on

May, 17, 2022 (Tuesday), 3:00 pm

Venue
IEE Department Seminar Room (3rd Floor), Salt Lake Campus

Abstract:
Today we are seeing significant interest for the adoption of wide band gap devices in several power electronics sectors. In the UK, the power electronics supply chain contributes approximately £49Bn to GDP, employs 82,000 high-value jobs in design and manufacture, and approximately 95% of power electronics designed in the UK goes to export. By 2026, the convertor market for EV's is estimated to reach $19.5B, and the market for power semiconductors will be $5.6Bn. Wide band gap devices (e.g., Silicon Carbide, Gallium Nitride, etc.) provide significant opportunities for the power electronics industry. Compared to silicon, they have faster switching frequencies, better heat dissipation, and can operate at higher temperatures. But, WBG devices pose several challenges in terms of their packaging.

This presentation will discuss developments in packaging technology for wide-band gap devices. Thermo-mechanical analysis of these packages will also be demonstrated to illustrate optimal package architectures and interconnect structures and die-attach material (solder and sintered silver). The behavior of wide-band gap devices in a press-pack power module construction will also be discussed. For such a construction, the choice of contact pad material can be important. The presentation will compare both molybdenum and aluminium graphite as choices for contact pad materials, and demonstrate their impact on both thermal and thermo-mechanical performance. In summary, innovative solutions will be required in packaging designs to support growth in applications of wide band gap devices.

Bio-sketch

Chris Bailey is Junior-Past President of the IEEE Electronics Packaging Society and Director of the Computational Mechanics and Reliability Group at the University of Greenwich, UK. He has a PhD in Computational Modelling and an MBA in Technology Management and has published over 300 papers on Design and Simulation of Electronics Packaging. Chris has served on several external government committees, which include the 2014 UK Research Excellence Framework to assess research outputs and research impact across UK universities. He is a member of the EPSRC College (UK Equivalent to NSF in the USA) and associate editor for the IEEE Transactions of Components, Packaging, and Manufacturing Technology. He is also co-chair for the modelling and simulation technical working group on the IEEE Heterogeneous Integration Roadmap.

1. **Course Fee:** Nil
2. **Eligibility:** ME and PhD Students and Faculty. Undergraduate students interested in this field also can participate
3. **Registration:** Through e-mail to the coordinator at or spot registration on the day.
4. **For further details:** Contact the Course Coordinator, Prof. Ranjan Ganguly, Power Engineering Department, Jadavpur University (ranjan.ganguy@jadavpuruniversity.in)